

**AMENDMENTS TO THE CLAIMS**

Please amend claims 23, 24, 34 and 41-43 as follows:

1.-13. (canceled)

14. (Previously Presented) A method of manufacturing a semiconductor device according to claim 23, further comprising:

forming a passivation film on the third interlayer insulating film, the passivation film exposing the bonding pad.

15. (Previously Presented) A method of manufacturing a semi conductor device according to claim 14, wherein the passivation film is formed by forming a silicon oxide film and a silicon nitride film.

16. (Previously Presented) A method of manufacturing a semiconductor device according to claim 23, wherein the step (c) of forming the first interlayer insulating film comprises:

forming a first silicon oxide film;

coating hydrogen silsesquioxane resin to form a ceramic silicon oxide film; and

forming a second silicon oxide film on the ceramic silicon oxide film by plasma CVD.

17. (Original) A method of manufacturing a semiconductor device according to claim 16, further comprising a step of planarizing the second silicon oxide film by CMP.

18. (Original) A method of manufacturing a semiconductor device according to claim 16, further comprising a step of planarizing the second silicon oxide film by etching.

19. (Previously Presented) A method of manufacturing a semiconductor device according to claim 23, wherein the step (c) comprises of:

- forming Ti films covering inner surfaces of the through holes in the first interlayer insulating film of the base layer;
- forming TiN layers on the Ti films; and
- forming W layers on the TiN layers.

20. (Previously Presented) A method of manufacturing a semiconductor device according to claim 23, wherein the step (c) comprises:

- forming Ti films covering inner surfaces of the through holes in the first interlayer insulating film by sputtering;
- forming TiN layers on the Ti films by sputtering; and
- forming W layers on the TiN layers.

21. (Previously Presented) A method of manufacturing a semiconductor device according to claim 23, wherein the step (c) comprises:

- forming Ti films covering inner surfaces of the through holes in the first interlayer insulating film;
- forming TiN layers on the Ti films; and
- forming W layers on the TiN layers by plasma CVD.

22. (Previously Presented) A method of manufacturing a semiconductor device according to claim 23, wherein the step (b) of forming the first conductive pad comprises:

- forming a Ti layer;
- forming an Al-Cu alloy layer;
- forming a Ti layer; and
- forming a TiN layer.

23. (Currently Amended) A method of manufacturing a semiconductor device, the method comprising the steps of:

- (a) forming an insulating film on a semiconductor substrate;
- (b) simultaneously forming a first conductive pad and a first wiring layer on the insulating film;
- (c) forming a first interlayer insulating film on the first conductive pad, the first wiring layer and the insulating film;
- (d) forming a plurality of first through holes in the first interlayer insulating film, each of the first through holes extending from the first conductive pad or the first wiring layer respectively, to an upper surface of the first interlayer insulating film;
- (e) filling the plurality of first through holes with conductive material;
- (f) simultaneously forming a second conductive pad and a second wiring layer on the first interlayer insulating film, each of the second conductive pad and the second wiring layer being in contact with the conductive material in one or more of the plurality of first through holes;
- (g) forming a second interlayer insulating film on the second conductive pad, the second wiring layer and the first interlayer insulating film;
- (h) forming a plurality of second through holes in the second interlayer insulating film, each of the second through holes extending from the second conductive pad or the second wiring layer, respectively, to an upper surface of the second interlayer insulating film;
- (i) filling the plurality of second through holes formed in the second interlayer insulating film with conductive material;
- (j) simultaneously forming a third conductive pad and a third wiring layer on the second interlayer insulating film, each of the third conductive pad and wiring layer being in contact with the conductive material in one or more of the second through holes formed in the second interlayer insulating film;

(k) forming a third interlayer insulating film on the third conductive pad, the third wiring layer and the second interlayer insulating film;

(l-1) forming ~~a through hole~~, through the third interlayer insulating film, a third through hole above the third wiring layer and a through aperture above the third conductive pad which is substantially ~~the same size as the third conductive pad wider than~~ said third through hole;

(l-2) ~~forming~~ simultaneously filling said third through hole with a conductive material and leaving a conductive ~~portion~~ material covering a side wall of the through ~~hole~~ through the third interlayer insulating film aperture so that part of the third conductive pad is exposed; and

(m) simultaneously forming an uppermost wiring layer in contact with the conductive material in said third through hole and a bonding pad on the third conductive pad in the through hole aperture, in the third interlayer insulating film.

24. (Currently Amended) A method of manufacturing a semiconductor device, the method comprising the steps of:

(a) forming an insulating film on a semiconductor substrate;

(b) forming a base layer over the insulating film by carrying out at least the following acts:

(1) simultaneously forming a conductive pad and a wiring layer on the insulating film;

(2) forming a base layer insulating film on the conductive pad, the wiring layer and the insulating film;

(3) forming a plurality of base through holes in the base layer insulating film, each of the through base holes extending from the conductive pad or the wiring layer, respectively, to an upper surface of the base layer insulating film;

(4) filling the base through holes with a conductive material;

(c) forming first through nth intermediate layers over the base layer, n being a positive integer greater than 1, the first intermediate layer being formed on the base layer, the remaining intermediate layers being formed one on top of the other, each of the respective intermediate layers being formed by carrying out at least the following steps:

(1) simultaneously forming a conductive pad and a wiring layer on the insulating film of the immediately preceding layer, each of the conductive pad and wiring layer being in contact with the conductive material in one or more of the through holes of the immediately preceding layer;

(2) forming a respective interlayer insulating film on the conductive pad, the wiring layer and the insulating film of the immediately preceding layer;

(3) forming a plurality of through holes in the interlayer insulating film of the respective intermediate layer, each of the through holes extending from the conductive pad or wiring layer, respectively, of the respective intermediate layer to an upper surface of the interlayer insulating film of the respective intermediate layer;

(4) filling each of the through holes of the respective intermediate layer with a conductive material; and

(d) forming an upper layer on the nth intermediate layer by carrying out at least the following steps:

(1) ~~simultaneously forming a conductive pad and a wiring layer on the interlayer insulating film of the nth intermediate layer, each of the conductive pad and wiring layer being in contact with the conductive material in that plurality of one or more of the through holes in the insulating film of the nth intermediate layer which are in contact with the conductive pad of the nth intermediate layer;~~

(2) forming an upper layer insulating film on both the conductive pad ~~and the wiring layer~~ of the upper layer and the insulating film of the nth intermediate layer;

(3-a) forming ~~an upper through hole, through the upper layer insulating film, the upper through hole being substantially the same size as the conductive pad~~

~~of the upper layer~~ an upper through hole above the wiring layer of the upper layer  
and a through aperture above the conductive pad of the upper layer, the through  
aperture being substantially wider than said upper through hole;

(3-b) ~~forming~~ simultaneously filling said upper through hole with a  
conductive material and leaving a conductive portion material covering a side wall of  
the upper through hole aperture so that part of the conductive pad of the upper  
layer is exposed; and

(4) simultaneously forming an uppermost wiring layer connected to the  
conductive material in said upper through hole, and a bonding pad on the  
conductive pad of the upper layer, the bonding pad being located in the upper  
through hole aperture in the upper layer insulating film.

25. (Previously Presented) A method of manufacturing a semiconductor device  
according to claim 24, further comprising:

(e) forming a passivation film on the upper layer insulating film, the passivation  
film exposing the bonding pad.

26. (Previously Presented) A method of manufacturing a semiconductor device  
according to claim 25, wherein the passivation film is formed by forming a silicon oxide  
film and a silicon nitride film.

27. (Previously Presented) A method of manufacturing a semiconductor device  
according to claim 24, wherein the step (b)(2) of forming the base layer insulating film  
comprises:

forming a first silicon oxide film;  
coating hydrogen silsesquioxane resin on the silicon oxide film;  
thermally treating the hydrogen silsesquioxane to form a ceramic silicon oxide  
film; and

forming a second silicon oxide film on the ceramic silicon oxide film by plasma CVD.

28. (Previously Presented) A method of manufacturing a semiconductor device according to claim 27, further comprising a step of planarizing the second silicon oxide film by CMP.

29. (Previously Presented) A method of manufacturing a semiconductor device according to claim 27, further comprising a step of planarizing the second silicon oxide film by etching.

30. (Previously Presented) A method of manufacturing a semiconductor device according to claim 24, wherein the step (b)(4) comprises:

forming Ti films covering an inner surface of the through holes in the base layer insulating film;

forming TiN layers on the Ti films; and

forming W layers on the TiN layers.

31. (Previously Presented) A method of manufacturing a semiconductor device according to claim 24, wherein the step (b)(4) comprises:

forming Ti films covering an inner surface of the through holes in the base layer insulating film by sputtering;

forming TiN layers on the Ti films by sputtering; and

forming W layers on the TiN layer.

32. (Previously Presented) A method of manufacturing a semiconductor device according to claim 24, wherein the step (b)(4) comprises:

forming Ti films covering an inner surface of the through holes in the base layer insulating film;

forming TiN layers on the Ti films; and

forming W layers on the TiN layer by blanket CVD.

33. (Previously Presented) A method of manufacturing a semiconductor device according to claim 24, wherein the step (c)(1) of forming the conductive pad comprises:

forming a Ti layer;

forming an Al-Cu alloy layer;

forming a Ti layer; and

forming a TiN layer.

34. (Currently Amended) A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a multi-level sub-structure on an underlying insulating layer which is formed over a semiconductor substrate by repeating the steps of;

(1) forming a conductive layer;

(2) patterning the conductive layer to leave a wiring region and a pad region;

(3) forming an insulating layer over the patterned wiring and pad regions;

(4) forming a wiring via hole through the insulating layer above the wiring region and a plurality of pad via holes through the insulating layer above the pad region;

(5) embedding the via holes with conductive material to form a wiring via connected to the wiring region and a plurality of pad vias connected to the pad region;

(b) forming an upper conductive layer on a surface of the multi-level sub-structure;

(c) patterning the upper conductive layer to leave an upper wiring region and an upper pad region;

(d) forming an upper insulating layer over the upper wiring region and the upper pad region;



(e-1) forming ~~an upper wiring via hole~~, through the upper insulating layer, ~~an upper wiring via hole~~ above the upper wiring region ~~so as to form~~ and an opening which ~~exposes a central region of~~ above the upper pad region encompassing a region above said plurality of pad vias;

(e-2) simultaneously filling said upper wiring via hole with a conductive material, and ~~leaving forming a conductive portion material~~ covering a side wall of the ~~upper wiring via hole opening~~ so that part of the upper pad region is exposed; and

(f) simultaneously forming an uppermost wiring region connected to the conductive material in said upper wiring region via hole and an uppermost pad region connected to said upper pad region, wherein the wiring regions and the pad regions are respectively vertically registered.

35. (Previously Presented) A method of manufacturing a semiconductor device, the method comprising the steps of:

- (a) forming an insulating film on a semiconductor substrate;
- (b) forming a first conductive pad on the insulating film;
- (c) forming a first interlayer insulating film on both the first conductive pad and the insulating film;
- (d) forming a plurality of first through holes in the first interlayer insulating film extending from the first conductive pad to an upper surface of the first interlayer insulating film;
- (e) filling the plurality of first through holes with conductive material;
- (f) forming a second conductive pad on the first interlayer insulating film in contact with the conductive material in the plurality of first through holes;
- (g) forming a second interlayer insulating film on both the second conductive pad and the first interlayer insulating film;

(h) forming a plurality of second through holes in the second interlayer insulating film extending from the second conductive pad to an upper surface of the second interlayer insulating film;

(i) filling the plurality of second through holes formed in the second interlayer insulating film with conductive material;

(j) forming a third conductive pad on the second interlayer insulating film and in contact with the conductive material in the second through holes formed in the second interlayer insulating film;

(k) forming a third interlayer insulating film on both the third conductive pad and the second interlayer insulating film;

(l) forming a through hole through the third interlayer insulating film which is substantially the same size as the third conductive pad; and

(m) forming a bonding pad on the third conductive pad in the through hole in the third interlayer insulating film,

wherein the step (c) of forming the first interlayer insulating film comprises:

forming a first silicon oxide film;

coating hydrogen silsesquioxane resin on the first silicon oxide film;

thermally treating the hydrogen silsesquioxane resin to form a ceramic silicon oxide film; and

forming a second silicon oxide film on the ceramic silicon oxide film by plasma CVD.

36. (Previously Presented) A method of manufacturing a semiconductor device according to claim 35, further comprising a step of planarizing the second silicon oxide film by CMP.

37. (Previously Presented) A method of manufacturing a semiconductor device according to claim 35, further comprising a step of planarizing the second silicon oxide film by etching.

38. (Previously Presented) A method of manufacturing a semiconductor device, the method comprising the steps of:

(a) forming an insulating film on a semiconductor substrate;  
(b) forming a base layer over the insulating film by carrying out at least the following acts:

(1) forming a conductive pad on the insulating film;  
(2) forming a base layer insulating film on both the conductive pad and the insulating film;  
(3) forming a plurality of base through holes in the base layer insulating film which through holes extend from the conductive pad to an upper surface of the base layer insulating film;

(4) filling the base through holes with a conductive material;  
(c) forming first through nth intermediate layers over the base layer, n being a positive integer greater than 1, the first intermediate layer being formed on the base layer, the remaining intermediate layers being formed one on top of the other, each of the respective intermediate layers being formed by carrying out at least the following steps:

(1) forming a conductive pad on the insulating film of the immediately preceding layer in contact with the conductive material in the through holes of the immediately preceding layer;

(2) forming a respective interlayer insulating film on both the conductive pad and the insulating film of the immediately preceding layer;

(3) forming a plurality of through holes in the interlayer insulating film of the respective intermediate layer, the through holes extending from the conductive pad of the respective intermediate layer to an upper surface of the interlayer insulating film of the respective intermediate layer;

(4) filling each of the through holes of the respective intermediate layer with a conductive material; and

(d) forming an upper layer on the nth intermediate layer by carrying out at least the following steps:

(1) forming a conductive pad on the interlayer insulating film of the nth intermediate layer in contact with the conductive material in the plurality of through holes in the insulating film of the nth intermediate layer;

(2) forming an upper layer insulating film on both the conductive pad of the upper layer and the insulating film of the nth intermediate layer;

(3) forming an upper through hole through the upper layer insulating film, said upper through hole being substantially the same size as the conductive pad of the upper layer; and

(4) forming a bonding pad on the conductive pad of the upper layer, the bonding pad being located in the upper through hole in the upper layer insulating film,

wherein the step (b)(2) of forming the base layer insulating film comprises:

forming a first silicon oxide film;

coating hydrogen silsesquioxane resin on the silicon oxide film;

thermally treating the hydrogen silsesquioxane to form a ceramic silicon oxide film; and

forming a second silicon oxide film on the ceramic silicon oxide film by plasma CVD.

39. (Previously Presented) A method of manufacturing a semiconductor device according to claim 38, further comprising a step of planarizing the second silicon oxide film by CMP.

40. (Previously Presented) A method of manufacturing a semiconductor device according to claim 38, further comprising a step of planarizing the second silicon oxide film by etching.

41. (Currently Amended) A method of manufacturing a semiconductor device according to claim 23, wherein the ~~sidewall lamination include~~ conductive portion includes Ti, TiN and W layers.

42. (Currently Amended) A method for manufacturing a semiconductor device according to claim 24, wherein the ~~sidewall lamination include~~ conductive portion includes Ti, TiN and W layers.

43. (Currently Amended) A method of manufacturing a semiconductor device according to claim 34, wherein the ~~sidewall lamination include~~ conductive portion includes Ti, TiN and W layers.

44. (Previously Presented) A method of manufacturing a semiconductor device according to claim 23, wherein the conductive portion formed in step (1-2) is formed to cover the entire side wall of the through hole.

45. (Previously Presented) A method of manufacturing a semiconductor device according to claim 23, wherein the step (1-2) comprises forming a conductive layer on the third interlayer insulating film and etching the conductive layer to leave the conductive portion on the side wall of the through hole.

46. (Previously Presented) A method of manufacturing a semiconductor device according to claim 45, wherein the step (1-1) also forms a third through hole through the third interlayer insulating film on the third wiring layer, and the step (1-2) forms a conductive filler in the third through hole.

47. (Previously Presented) A method of manufacturing a semiconductor device according to claim 24, wherein the conductive portion formed in step (d)(3-b) is formed to cover the entire side wall of the through hole.

48. (Previously Presented) A method of manufacturing a semiconductor device according to claim 24, wherein the step (d)(3-b) comprises forming a conductive layer on the third interlayer insulating film and etching the conductive layer to leave the conductive portion on the side wall of the through hole.

49. (Previously Presented) A method of manufacturing a semiconductor device according to claim 48, wherein the step (d)(3-a) also forms a third through hole through the third interlayer insulating film on the third wiring layer, and the step (d)(3-b) forms a conductive filler in the third through hole.

50. (Previously Presented) A method of manufacturing a semiconductor device according to claim 34, wherein the conductive portion formed in step (e-2) is formed to cover the entire side wall of the through hole.

51. (Previously Presented) A method of manufacturing a semiconductor device according to claim 34, wherein the step (e-2) comprises forming a conductive layer on the third interlayer insulating film and etching the conductive layer to leave the conductive portion on the side wall of the through hole.

52. (Previously Presented) A method of manufacturing a semiconductor device according to claim 51, wherein the step (e-1) also forms a third through hole through the third interlayer insulating film on the third wiring layer, and the step (e-2) forms a conductive filler in the third through hole.